

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A record carrier ~~(1)~~of a recordable or rewritable type for storing information according to a standardized format defining parameters for such record carriers, the record carrier comprising pre-recorded address information ~~(4,5,6,8)~~in a preformed track comprising:

address data bits ~~(4,5,6)~~indicating a current position of the address information in the preformed track on the record carrier, the address data bits being arranged ~~according to~~in accordance with the said standardized format, and

pre-recorded error-protection parity bits (8)~~for detecting enabling a recording device to detect errors in the~~ address data,

~~which characterized in that the pre-recorded error-protection parity bits are arranged to deviate from the error-protection parity bits according to~~in accordance with the said standardized format thereby resulting in incorrect detection of errors in the address data by a recording device in accordance with said standardized format.

2. (Currently Amended) A ~~The~~record carrier according to~~as claimed in~~ claim 1, wherein the error-protection parity bits ~~(8)~~ are being calculated using a check polynomial ~~(P)~~that deviates

from the check polynomial ~~according to~~ in accordance with the said standardized format.

3. (Currently Amended) A ~~The~~ record carrier ~~according to~~ as claimed in claim 2, wherein ~~the said~~ standardized format is the CD-R format, and the check polynomial ~~(P)~~ used is:

$$P(X) = X^{14} + X^{12} + X^{11} + X^{10} + X^4 + X^3 + X^2 + 1.$$

4. (Currently Amended) A ~~The~~ record carrier ~~according to~~ as claimed in claim 1, wherein ~~the said~~ standardized format is the CD-R format, and not all the error-protection parity bits ~~(9)~~ are inverted.

5. (Currently Amended) A ~~The~~ record carrier ~~according to~~ as claimed in claim 4, wherein the first ten error-protection parity bits are inverted and the last four error-protection parity bits are non-inverted.

6. (Currently Amended) A ~~The~~ record carrier ~~according to~~ as claimed in claim 1, wherein the address information ~~(4,5,6,8)~~ is ~~recorded pre-recorded in the preformed track~~ on the record carrier by wobbling a pre-groove ~~(2)~~ forming the preformed track.

7. (Currently Amended) A ~~The~~ record carrier ~~according to~~ as claimed in claim 1, wherein the address information ~~(4,5,6,8)~~ are

~~recorded~~ is pre-recorded in the preformed track on the record carrier as pre-pits.

8. (Currently Amended) A device ~~(9)~~ for storing information on the record carrier ~~(1)~~ according to as claimed in claim 1, said device comprising:

_____ reading means ~~(10)~~ for reading the pre-recorded address data bits ~~(4,5,6)~~ and the pre-recorded error-protection parity bits ~~(8)~~ present from the preformed track on the record carrier,;

_____ error-detection means ~~(12)~~ for detecting errors in the address information; and

_____ writing means ~~(10)~~ for storing information on the record carrier,

wherein the error-detection means ~~(12)~~ are adapted for detecting ~~detects~~ the errors in the address data bits ~~(4,5,6)~~ using the error-protection parity bits ~~(8)~~ that arranged to deviate from the error-protection parity bits according to in accordance with the said standardized format.

9. (Currently Amended) A ~~The device according to as claimed in claim 8, wherein the error-detection means (12) are adapted for detecting~~ detects the errors in the address information using a check polynomial that deviates from the check polynomial ~~according to in accordance the said standardized format.~~

10. (Currently Amended) ~~A~~ The device according to ~~as claimed in~~
claim 9, wherein ~~the~~ said standardized format is the CD-R format,
and the check polynomial ~~(P)~~ used is:

$$P(X) = X^{14} + X^{12} + X^{11} + X^{10} + X^4 + X^3 + X^2 + 1.$$

11. (Currently Amended) ~~A~~ The device according to ~~as claimed in~~
claim 8, wherein ~~the~~ said standardized format is the CD-R format,
and not all the error-protection parity bits ~~(9)~~ are inverted.

12. (Currently Amended) ~~A~~ The device according to ~~as claimed in~~
claim 11, wherein the first ten error-protection parity bits are
inverted and the last four error-detection data bits are non-
inverted.